

IN THE CLAIMS

Please cancel claims 2 and 5-9 without prejudice, amend claims 1, 3-4 and 10, and add claims 11-21 as follows:

1 1. (Currently amended) A rate matching circuit for adjusting
2 the number of bits in a data block, the data block comprising a
3 plurality of interleaved words generated by the action of an
4 interleaving circuit on a coded output generated by the action of a
5 coding circuit on a digital input, the coded output having a
6 greater number of bits than the digital input, the rate matching
7 circuit having means for adjusting the number of bits in the data
8 block using a rate matching pattern to provide data bits for
9 transmission during respective frames of a transmission channel,
10 ~~characterised in that~~ and ~~means are provided for selecting the rate~~
11 ~~matching pattern depending on the characteristics of the coding~~
12 ~~circuit and of the interleaving circuit~~ a bit deletion/repetition
13 rate, wherein a bit deletion/repetition pattern is selected to
14 ensure that the deleted or repeated bits are not required to enable
15 all bits from the digital input to be reconstructed.

2. (Canceled)

1 3. (Currently amended) A rate matching circuit as claimed in
2 claim 1 ~~or 2, characterised in that~~, wherein the rate matching
3 pattern for each interleaved word within the data block is offset
4 with respect to the adjacent interleaved word or words within the
5 block.

1 4. (Currently amended) A rate matching circuit as claimed in
2 ~~any one of claims 1 to 3, characterised in that~~, wherein the rate
3 matching pattern is selected as a function of the interleaving
4 depth of the interleaving circuit.

Claims 5-9. (Canceled)

1 10. (Currently amended) A method of operating a rate matching
2 circuit to adjust the number of bits in a data block, the data
3 block comprising a plurality of interleaved words generated by the
4 action of an interleaving circuit on a coded output generated by
5 the action of a coding circuit on a digital input, the coded output
6 having a greater number of bits than the digital input, the rate
7 matching circuit adjusting the number of bits in the data block
8 using a rate matching pattern to provide data bits for transmission

9 during respective frames of a transmission channel, characterised
10 ~~by and~~ selecting the rate matching pattern depending on the
11 ~~characteristics of the coding circuit and of the interleaving~~
12 ~~circuit~~ a bit deletion/repetition rate, wherein a bit
13 deletion/repetition pattern is selected to ensure that the deleted
14 or repeated bits are not required to enable all bits from the
15 digital input to be reconstructed.

1 11.(New) The rate matching circuit of claim 1, wherein the
2 rate matching pattern forms a matrix including change bits that
3 indicate change of corresponding bits of said interleaved words
4 within said data block, wherein each row of said matrix includes a
5 maximum of one of said change bits.

1 12.(New) The rate matching circuit of claim 1, wherein said
2 coding circuit has one of a fixed code rate and a predetermined
3 number of rates for a variable data source.

1 13.(New) The rate matching circuit of claim 1, wherein said
2 interleaving circuit is not adaptive.

1 14.(New) The rate matching circuit of claim 1, wherein said
2 interleaving circuit has a constant bit rate.

1 15.(New) The rate matching circuit of claim 1, wherein said
2 coding circuit has one of a fixed code rate and a predetermined
3 number of rates for a variable data source, and wherein said
4 interleaving circuit is not adaptive.

1 16.(New) The rate matching circuit of claim 1, wherein said
2 rate matching circuit alters a coding rate of said coding circuit.

1 17.(New) The method of claim 10, wherein change bits of said
2 rate matching pattern for deleting or repeating bits of said data
3 block are offset with respect to the each other.

1 18.(New) The method of claim 10, wherein change bits of said
2 rate matching pattern for deleting or repeating bits of said data
3 block are offset with respect to the each other along adjacent
4 columns of a matrix of said rate matching pattern.

1 19.(New) The method of claim 10, wherein change bits of said
2 rate matching pattern for deleting or repeating bits of said data

3 block are offset with respect to the each other along adjacent rows
4 of a matrix of said rate matching pattern.

1 20.(New) The method of claim 10, wherein change bits of said
2 rate matching pattern for deleting or repeating bits of said data
3 block are offset with respect to the each other along adjacent rows
4 and columns of said rate matching pattern.

1 21.(New) The method of claim 10, wherein said interleaving
2 circuit forms said data block by filling a matrix row by row with
3 row bits of said coded output and outputs column bits of said
4 matrix column by column to form said interleaved words.